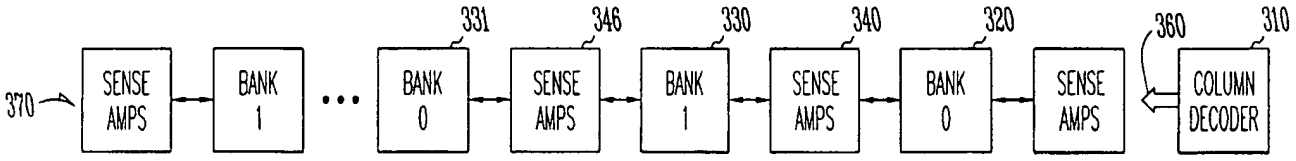
## REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on March 20, 2003, and the references cited therewith. In response thereto, Applicant submits the following remarks in support of patentability without amendment to the claims or to the application. Reconsideration of the claims, removal of the rejections and allowance of all claims is respectfully solicited.

*In the Drawings*

The drawings were objected to under 37 C.F.R. 1.83(a) since the drawings allegedly did not show every feature of the invention specified in the claims. The feature of the memory cores from two of the different ones of the plurality banks are interleaved in a strip with the plurality of shared sense amplifiers as recited in claims 1-60 and their connective relationship is alleged to be missing.

As described in connection with the argument against the rejections under 35 U.S.C. § 112, second paragraph, stated below, Applicant maintains that the strip 370 and the connective relationships are already shown in Figure 3.




Viewing strip 370 from left to right in Figure 3 (duplicated above), one finds a sense amplifier on the far left connected with a double-headed arrow to a box containing some memory cores or cells of BANK 1. The connective relationship is indicated by the double-headed arrow which in electrical schematic diagrams indicates a two-way communication path.

Looking again to strip 370 of Figure 3, BANK 1 is followed by an ellipses indicating a portion of the strip is missing for an abbreviated description. Following the ellipses is another box containing memory cores or cells of BANK 0 in a box labeled 331, followed by a connective arrow between box 331 and sense amplifier box 346, followed another connective arrow, followed by more memory cores for BANK 1 in a box labeled 330. The connective relationships between the sense amplifier in box 346 and BANK 0 (to the left) and BANK 1 (to the right) is shown with the double-

headed arrows between the boxes. This indicates that sense amplifier 346 can serve both the cores in box 331 (of BANK 0) or the cores in box 330 (of BANK 1).

Continuing to view strip 370 from left to right, the memory cores of BANK 1 in box 330 are also connected through an arrow to box 340 which is another sense amplifier. This sense amplifier 340 is also connected to more memory cores of BANK 0 in box 320 through another double-headed arrow. This arrow indicates that sense amplifier 340 can serve both the cores in box 330 (of BANK 1) and the cores in box 320 (of BANK 0).

When viewing strip 370 from left to right, one finds an alternating pattern: cores from BANK 1 connected to a sense amplifier, which is connected to cores from BANK 0, which is connected to another sense amplifier, which is connected to cores from BANK 1, which is connected to another sense amplifier, which is connected to cores from BANK 0, etc. This is called interleaving along strip 370: BANK 1 – BANK 0 – BANK 1 – BANK 0 – BANK 1 – etc. The memory cores alternate between the two memory banks.

Applicant submits that the drawings already show the features of claims 1-60 and respectfully request removal of the objection to the drawings.

*§112 Rejection of the Claims*

Claims 1-60 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses this rejection since the claimed interleaving connective relationship between the memory cores is already shown in Figure 3.

Figure 3 already shows a strip 370 in which the memory cores 320 from BANK 0 shares sense amplifier 340 with the memory cores 330 of BANK 1. Also, Figure 3 already shows in strip 370 the memory cores 330 from BANK 1 sharing sense amplifier 346 with the memory cores 331 of BANK 0. This is an interleave: BANK 0, BANK 1, BANK 0, etc. The connective relationship is shown by double-headed arrows between the boxes. Also, the column decode lines are shown to traverse the entire row with a larger arrow 360, accompanied by the following text taken from the patent application specification beginning on page 6, line 13:

> Column decode lines driven by column decoders typically traverse an entire row of memory cores, rather than only memory cores nearby. For example, column decoder 310 drives column decode lines 360 shown schematically in Figure 3 as an arrow. One or more of column decode lines 360 traverse multiple memory cells of the row to enable sense amplifiers within the row across from the column decoder. For example, a column decode line that enables sense amplifiers 346 to read from memory core 331 in Bank 0 will typically travel over, under, or past memory cores 320 and 330 from Banks 0 and 1, respectively.

Not all elements of the drawing need to be shown according to 37 C.F.R. § 1.83(a):

> The drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box).

In the present patent application, the interleaving of memory cores from different memory banks is shown in Figure 3. The connective relationship is shown with arrows between the boxes. A large arrow 360 shows the global nature of the column decoder. Applicant therefore can find no shortcomings in the drawings. Applicant respectfully requests withdrawal of the rejection of claims 1-60.

*§103 Rejection of the Claims*

Claims 1-56 (*sic*, read 1-60) were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohsawa (U.S. 5,970,016) in view of Morton (U.S. 5,159,572). Applicant respectfully traverses this rejection on several grounds described below. For the reasons stated, Applicant has deemed that the claims still do not require amendment since they already distinguish over the art of record.

All Elements of the Claims are not Present in the Combination

The Ohsawa patent describes a DRAM device with memory banks capable of independent operation, such as Rambus and the like. (Ohsawa, col. 1, lines 7). This architecture is similar to the architecture shown in Applicant's patent application in conjunction with Figure 1. As a result of this

architecture, the Ohsawa patent suffers from the same noise problems in Multi-bank operation as described by Applicant in conjunction with Figure 1. However, Ohsawa does not recognize the problem or provide a solution for the sense amplifier noise resulting from adjacent column decode lines being active at the same time during simultaneous multi-bank operation.

The Morton patent describes a very old DRAM architecture which uses distributed row address decode and uses interleaved word line signals in a cell array. For example, Figure 3 of the Morton patent shows cell array 26 having rows of cells being address from both word line decode units 48 and 48' (see arrows alternating in left and right directions). This use of the term "interleaving" refers only to local word lines and has nothing to do with alternating banks of memory. Further, the Morton patent describes a traditional DRAM from approximately 13 years ago which was not capable of simultaneous access of multiple banks of memory such as the type found in the Ohsawa patent. Hence, the Morton patent fails to teach an interleaving of different ones of a plurality of banks in a strip with shared sense amplifiers. Morton also fails to describe sense amplifiers which are shared between banks of memory (there are no banks of memory in Morton). Morton and Ohsawa also fail to even identify any noise problems in sense amplifiers associated with multiple memory bank access.

Since all of the elements of the claimed invention are not found in the combination of references cited in the First Office Action, the rejection of claims 1-60 under 35 U.S.C. §103(a) must fail. Applicant respectfully requests reconsideration of the claims and allowance of all claims.

The Motivation to Combine is Nowhere Taught in the Combination

Applicant has identified a potentially serious problem associated with simultaneous multi-bank access in Rambus-type architecture. Noise from adjacent firing column decoder lines can have an adverse impact on proper sensing in sense amplifiers.

To arrive at the Applicant's claimed invention by combining the Ohwasa and Morton patents as proposed by the examiner, one of ordinary skill in the art would have had to find the elements of the claims in the references *and* show the motivation to combine the references somewhere in the references themselves. Applicant respectfully submits that the examiner has not provided the required explanation as to why the applied prior art itself would have provided one of ordinary skill

in the art with a motivation to make this substitution and a reasonable expectation of success in doing so. *See In re Vaeck,* 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991); *In re O'Farrell,* 853 F.2d 894, 902, 7 USPQ2d 1673, 1680 (Fed. Cir. 1988).

The Examiner's argument that it would have been obvious under 35 U.S.C. § 103(a) for one of ordinary skill in the art at the time the invention was made to modify Figure 1 of Ohwasa by teaching as taught in Figure 3 of Morton "for the purpose of lower manufacturing cost and reliability" (citation to Morton, column 5, lines 64-68 and column 6, line 1-12) is not sufficient for carrying the burden of presenting a prima facia case of obviousness since the cited portion of Morton has nothing to do with the problem of noise identified by Applicant or the solution achieved. A broad conclusion that one skilled in the art would move in the technical direction of the present invention "to lower manufacturing cost" is not a motivation to combine the specific features of the two references to achieve the Applicant's claimed solution of reducing noise during simultaneous memory bank access.

For this and the other reasons cited above, Applicant respectfully requests reconsideration of the claims and allowance of all claims.

Examiner's Response to Applicant's Arguments

In the Final Office Action, the Examiner responded that Applicant's arguments were not persuasive. As to the drawings, Applicant has provided an exhaustive description of the interleaved interconnection as shown in Figure 3. As to the art rejections, the Examiner only addresses one of Applicant's arguments: that the references do not suggest the combination. The Examiner has ignored Applicant's other argument that the combination does not teach all of the elements of the claims.

For example, claims 1 reads as follows:

1. (Original) A memory device comprising:
a plurality of banks, each including a plurality of memory cores;
a plurality of sense amplifiers shared among memory cores of different ones of the plurality of banks; and
wherein the memory cores from two of the different ones of the plurality of banks are interleaved in a strip with the plurality of shared sense amplifiers.

The last paragraph of claim 1 requires that the memory cores be from two different memory banks and that they be interleaved with the sense amplifiers. In contrast to claims 1, the Morton patent only teaches the interleaving of word line, not memory cells in different memory banks. The other pending claims include similar limitations which are not found in the combination of references cited by the Examiner. Without all the elements of the claims found in the prior art references, the rejection of the claims under 35 U.S.C. § 103(a) fails. Reconsideration of claims 1-60 is respectfully solicited.

*Conclusion*

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney 612-373-6904 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date May 20, 2003

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 20th day of May, 2003

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Signature